

Partial Listing



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(54) SIMULTANEOUS MANUFACTURING AND PRODUCT ENGINEERING INTEGRATED WITH KNOWLEDGE NETWORKING

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(56) References Cited

U.S. PATENT DOCUMENTS

5,208,765	5/1993	Turnbull	700/97
5,257,363 *	10/1993	Shapiro et al.	703/13
5,307,261	4/1994	Maki et al.	700/95

5,355,317	10/1994	Talbott et al.	700/97
5,357,440	10/1994	Talbott et al.	700/97
5,640,337 *	6/1997	Huang et al.	703/23
5,748,943 *	5/1998	Kaepf et al.	703/1
5,752,000 *	5/1998	McGeer et al.	703/14
6,088,689 *	7/2000	Kohn et al.	706/10

* cited by examiner

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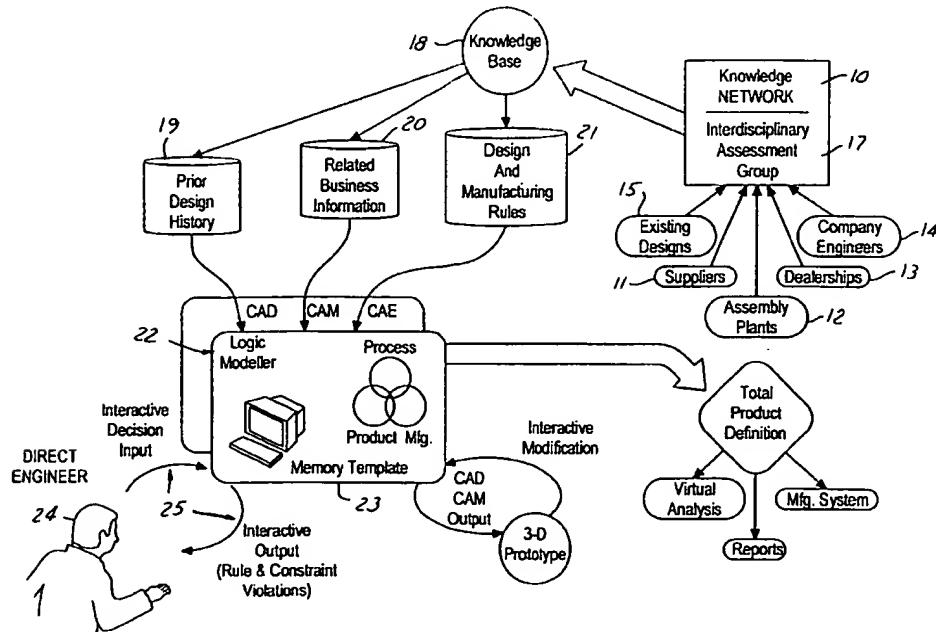
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(57) ABSTRACT

Method of simultaneously carrying out manufacturing and product engineering integrated with knowledge networking. The method comprises: (a) creating a logic modeller by (i) identifying elements of an engineering project and syntactically arranging such elements in a logic sequence based on engineering functions, (ii) ascertaining uniform meaning for such elements and engineering functions to allow for interdisciplinary communication, (iii) gathering existing knowledge pertinent to such elements and engineering functions, and encoding such gathered knowledge into terms according to uniform meanings, and (iv) programming a computer memory template with such logic sequence and with attached data bases of such encoded existing knowledge; and (b) operating said logic modeller through a direct engineer that: (i) requests review of initial input specifications of an inchoate design that results in an analysis by the modeller to indicate rule or constraint violations of the gathered knowledge, and (ii) interacts with the analysis in response to such indications to converge on acceptable or improved engineering design functions.

15 Claims, 9 Drawing Sheets



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Operating the logic modeller may start with selection of a points file in CAD and transporting such file into the modeller. Analysis by the modeller will present alternatives or suggested ways to overcome violations. If the first stages of interaction with the logic modeller does not result in a desired total product and manufacturing definition, the definition may be converted to a 3-D object for visual analysis so that the interactive step may be reiterated.

Before the final total product definition is reached, the direct engineer has the flexibility to interact with the developing inchoate design using a 3-dimensional prototype device that produces a physical specimen based on the modeller design file. In this way, the direct engineer can survey and further analyze the physical full sized product to see how it may function with associated elements or assemblies, and thus make other changes by modifying the design file (see FIG. 1).